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- Mentor Graphics Announces Revenues of $123M; Product Revenue Growth Rate Hits 25%, April 28, 1999
- Mentor Graphics Strengthens Management Team with Key Appointments, April 26, 1999
- LSI Logic Chooses Mentor Graphics in Contract for Design and Verification Tools, April 20,
- Mentor Graphics endorses New VHDL-AMS Standard For Rapid Growth of Mixed-Signal Systems-on-Chip Designs, April 5,
- Mentor Graphics and ARC Cores Partner to Deliver Emulation-Ready Processor Cores, April 7, *NOTE: The Celaro and SimExpress emulators are not being marketed or sold in the United States*

## March 1999

- Mentor Graphics Selects Benjamin Group and Shafer Advertising as Agency Partners to Strengthen Brand, March 30,
- Mentor Graphics Announces Availability of the Interconnectix Tool Suite on the Intel Architecture Windows NT Platform, March 22,
- Mentor Graphics Announces Ultra-High-Speed Capabilities for Next-Generation Personal Computer Motherboard Design, March 22,
- Mentor Graphics Announces Full System-Level Interconnect Simulation for Advanced Personal Computer Motherboard Design, March 22,
- Mentor Graphics and Zuken Announce Interoperability Agreement and Interface Availability, March 22,
- Mentor Graphics Turbo-charges Leading Calibre Tool: Multithreading Increases Performance Five to Six fold, March 22,
- Software Support Professional Association Awards Third STAR

Award to Mentor Graphics for Superior Support Services, March 17,

- Mentor Graphics Corporation Announces New Board Timing Solution That Cuts Weeks from Timing Verification Cycle, March 15,
- Model Technology Enhances Model*Sim*™ Simulator with Performance Analysis and Boost in RTL Performance, March 11,
- Mentor Graphics and ARM Announce New Hardware/Software Verification Solution for Embedded Systems, March 11, *NOTE: The Celaro and SimExpress emulators are not being marketed or sold in the United States*
- Platform Computing Forms Productivity Partnership With Mentor Graphics, March 11, *NOTE: The Celaro and SimExpress emulators are not being marketed or sold in the United States*
- Mentor Graphics Takes The Lead in HDL Design; Introduces Complete FPGA Flow, March 8,
- Mentor Graphics Provides PowerPC Developers with Complete Embedded Software Solution for Faster Design, March 1,

**February 1999**

- Mentor Graphics' Seamless Co-Verification Environment To Support Models Created Using CAE Plus' Model-Generation Tool for Toshiba's System-On-Chip Designs, February 24,
- Mentor Graphics Completes HDL Design Flow Picture; Brings Exemplar Logic In House, February 23,
- VLSI Endorses Mentor Graphics' Embedded Software Solution for System-on-Chip Design, February 22,
- Mentor Graphics Corporation Declares Dividend Distribution of Incentive Share Purchase Rights, February 10,
- Mentor Graphics Announces Record Fourth Quarter Revenues; Product Revenue up 38%, February 2,
- Mentor Graphics Introduces High-Performance Memory Generators, February 2,

**January 1999**

- Mentor Graphics and UMC Group Deliver Critical Support for 0.18-Micron Process, January 25,
- Model Technology Changes the Game in HDL Design, January 25,
- Model Technology First EDA Firm to Open E-Commerce Web Site, January 25,
- Mentor Graphics Calibre Physical Verification Sales Significantly Outpace Competitors, January 6,
- Mentor Graphics Pre-announces Record Fourth Quarter Revenues, Product Orders, and Gross Margin, January 5,
- Mentor Graphics Names New Vice President And General Manager of Microtec Division, January 4,

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PRESS RELEASE

**Model Technology Enhances Model*Sim*™ Simulator with Performance Analysis and Boost in RTL Performance**

**PORTLAND, Ore. - March 11, 1999:**

Model Technology Incorporated, a wholly owned subsidiary of Mentor Graphics Corporation (NASDAQ: MENT) and the leader in VHDL and mixed language simulation, today announced enhancements to its popular Model*Sim*™ Elite simulator. They include the addition of a performance analyzer, code coverage capability, and a Verilog register transfer level (RTL) performance improvement of up to five times the speed of previous Model*Sim* versions.

**Performance Analysis Unique in EDA**

Model*Sim* Elite version 5.3 has a built-in performance analyzer that identifies hardware description language (HDL) simulation bottlenecks. It works with VHDL and Verilog at all levels of abstraction. *ModelSim* is the only HDL simulator with performance analysis capability.

"Model*Sim*'s performance analyzer proved to be very effective because it gave our designers the ability to accelerate our high performance simulation environment," said Randy Dombrowski, CAE/design methodology manager at Real 3D, Inc., a leading provider of advanced computer graphics technology. "It gave us visibility into performance bottlenecks that enabled us to make modeling changes that significantly decreased our regression test time."

Performance results are shown in a hierarchical display enabling designers to quickly identify slow spots in their simulations. Armed with this information, design teams can make coding changes where they have the greatest impact, thereby reaping the benefits of faster simulation runs.

"Simulation performance is the name of the game in high-end ASIC design," said Dave Kresta, Model Technology product line manager. "Improvements can come from two sources—increasing the simulator's raw performance, and writing more efficient VHDL or Verilog code. Our experience shows that understanding the efficiency of code provides huge benefits in simulation. We've seen simulation performance increases of 10 times because of a few simple changes in coding style."

**RTL Verilog Performance Enhancements**

Model Technology has increased RTL Verilog performance by working with numerous customer designs. Depending upon their design styles, Model*Sim* Verilog users may experience speed increases of two to five times over previous versions of Model*Sim*. Model Technology continues to maintain its industry-leading compile times without designers having to change their coding and design styles.

**Code Coverage for Enhanced Efficiency**

Model*Sim*'s new integrated code coverage feature enhances overall efficiency of the verification environment by measuring the percentage of a HDL model exercised by a test bench during simulation. Code coverage provides a graphical summary of executable lines hit. The results can be accumulated during a set of regression tests. Users also can view the details of each source file.

**The First Language-Neutral Simulator**

The new ModelSim Elite simulator will include a language-neutral license enabling simulation of either VHDL or Verilog designs with one simulator and one license. Industry experts are predicting that single-language simulators will be replaced by simulators with single kernels within the next few years. Model Technology is the first company to deliver on this vision with single kernel architecture already powering its ModelSim tool.

**Pricing and Availability**

ModelSim Elite version 5.3 will be available in Q2 1999. The price will be $20,000. Existing customers will be notified of upgrade pricing.

**About Model Technology**

Model Technology Incorporated, a wholly owned subsidiary of Mentor Graphics Corporation, is the industry's leading supplier of HDL simulation tools. Model Technology provides ASIC and FPGA designers with the latest in simulation technology regardless of the language (VHDL, Verilog or mixed-HDL) or platform (Unix, NT) used. With more than 25,000 licensed units sold worldwide, Model*Sim* is the most popular HDL simulator in the industry. Model Technology is headquartered in Portland, Oregon, with 28 sales and distribution offices in the United States, Europe, Japan, and the Pacific Rim. For information on the nearest Model Technology representative or Model Technology products, call 503/641-1340, email sales@model.com, or visit http://web.archive.org/web/20000925204236/http://www.model.com/.

For more information, contact:

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**Sven Haarhoff**
Model Technology
(503) 526-1689
svenh@model.com

PRESS RELEASE

# VLSI Endorses Mentor Graphics' Embedded Software Solution for System-on-Chip Design; Licenses the XRAY Debugger for Multi-Core Debugging

**San Jose, CA, February 22, 1999** - Mentor Graphics Corporation (NASDAQ: MENT) Embedded Software Division today announced a technology licensing agreement under which VLSI Technology Inc. (NASDAQ: VLSI) will use its industry-leading XRAY® Debugger as the foundation for a new product aimed at software development and the verification of multi-core system-on-chip (SOC) designs.

Under the terms of the agreement, VLSI will distribute the Mentor Graphics XRAY Debugger as part of its new software development tool, JumpStart$_{XE}$ (XRAY-enabled), for simultaneous code generation and debugging for ARM, DSP and ARM/DSP multi-core applications. (See related announcement, "VLSI Announces JumpStart$_{XE}$ — A New Multi-Core Software Development Tool Suite," 2/22/99.)

This agreement extends the open architecture and productivity-enhancing features of the XRAY Debugger beyond traditional board-level embedded functions to the forefront of emerging SOC embedded applications. Designers working in a custom silicon environment can now use the proven multi-core debug methodology of the XRAY Debugger to meet their verification needs and help get new products to market more quickly.

"This relationship with VLSI greatly advances our goal of bringing comprehensive embedded software solutions to all designers working on SOC applications," said Michael Kaskowitz, vice president and general manager of Mentor Graphics' Embedded Software Division. "We can best serve this fast-growing design community by working with companies such as VLSI to provide turnkey verification solutions that enable designers to work at the system-level to produce high-quality products more quickly and cost-effectively."

"System-on-chip designers need access to tools that are flexible and capable of executing in multi-tasking environments," said Ray Slusarczyk, director of marketing for VLSI's Embedded Processor Division. "The Mentor Graphics XRAY Debugger provides a proven methodology for multi-core software debugging and is ahead of other debuggers we evaluated in overall quality and ease of use. We are excited to include this technology as part of our JumpStart$_{XE}$ product and expect it to be well received by our customers."

### Industry's Leading Debugger for SOC Verification

Mentor Graphics' industry-leading XRAY Debugger significantly reduces the amount of time needed to identify and resolve problems in multi-core SOC applications. It provides a common debugger interface for all stages of the embedded development process and supports all phases of embedded software for SOC design, including simulation, integration and hardware/software co-verification.

Through the Mentor Graphics Seamless Co-Verification Environment (CVE)$^{TM}$, the XRAY Debugger can be used to develop software and hardware in parallel, allowing users to verify system-level software, such as startup code and device drivers, against a gate-level simulation of the target hardware. Application development can proceed even when no hardware is available by using the XRAY Debugger with an Instruction Set Simulator. When connected to the final target hardware via the JTAG interface, the XRAY debugger can provide complete control over the processor, with zero target intrusion, ensuring rapid project completion and shortened time to market.

**About Mentor Graphics Corporation**

Mentor Graphics (Nasdaq: MENT) is a world leader in electronic hardware and software design solutions, providing products and consulting services for the world's largest electronic and semiconductor companies. Established in 1981, the company reported revenues over the last 12 months of $490 million and employs approximately 2,600 people worldwide. Company headquarters are located at 8005 S.W. Boeckman Road, Wilsonville, Oregon 97070-7777. World Wide Web site: http://www.mentor.com.

**About VLSI Technology**

VLSI Technology, Inc. designs and manufactures custom and semicustom integrated circuits for leading firms in the wireless communications, networking, consumer digital entertainment and computing markets. VLSI's value proposition is based on full-service customer support, deep libraries of vertical market-focused IC intellectual property, unparalleled custom circuit design expertise enabled through the Velocity Rapid Silicon Prototyping design style, and one of the world's most flexible and efficient custom circuit manufacturing facilities. The company is based in San Jose, California, with 1998 revenues from continuing operations of $547.8 million, and approximately 2,200 employees worldwide. Visit VLSI's homepage at http://web.archive.org/web/20000522185042/http://www.vlsi.com/.

Mentor Graphics Corporation (NASDAQ: MENT) is a world leader in electronic hardware and software design solutions, providing products and consulting services for the world's largest electronics and semiconductor companies. Established in 1981, the company reported revenues over the last 12 months of $468 million and employs approximately 2,500 people worldwide. Company headquarters are located at 8005 S.W. Boeckman Road, Wilsonville, Oregon 97070-7777.

###



Note to Editors: Mentor Graphics' Microtec Division has been renamed as Mentor Graphics' Embedded Software Division.

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lorie_bowlby@mentor.com

Sabina Burns
Director, Marketing Communications
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408/ 487-7125
sabina_burns@mentor.com

Product & Sales Information: 1-800-547-3000 or 1-503-685-8000
Corporate Headquarters: 1-800-592-2210 or 1-503-685-7000

PRESS R

# Model Technology First EDA Firm to Open E-Commerce Web Site

**Portland, Ore. — January 25, 1999** - Model Technology Incorporated, a wholly owned subsidiary of Mentor Gra Corporation (NASDAQ: MENT), and the leader in VHDL and mixed-HDL simulation, today announced the grand of its E-commerce Internet store. This marks the first step in the company's 1999 strategy to provide hardware description language (HDL) tools to *all* HDL designers. (See January 25, 1999 Press)

The full range of advanced and novice designers now can purchase Model Technology's leading simulation prod http://web.archive.org/web/20000925204020/http://www.model.com/.

"Our focus on efficiency has made us the price/performance leader of the industry," said John Ott, director of sal marketing, Model Technology. "Our online store makes buying ModelSim products more convenient and allows u deliver our world-class technology to a broader market at very competitive prices."

By expanding its multi-tier distribution network to include E-commerce, Model Technology is making its unique si kernel technology available to designers of less complex designs with prices beginning at $4,495.

**About Model Technology**

Model Technology Incorporated, a wholly owned subsidiary of Mentor Graphics Corporation, is the industry's lea supplier of HDL simulation tools. Model Technology provides ASIC and FPGA designers with the latest in simula technology regardless of the language (VHDL, Verilog or mixed-HDL) or platform (Unix, NT) used. With more tha 25,000 licensed units sold worldwide, Model*Sim* is the most popular HDL simulator in the industry. Model Techn headquartered in Portland, Oregon, with 28 sales and distribution offices in the United States, Europe, Japan, an Pacific Rim. For information on the nearest Model Technology representative or Model Technology products, call 503/641-1340, email sales@model.com, or visit http://web.archive.org/web/20000925204020/http://www.model.c

**For more information, contact:**

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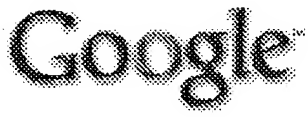

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- Try fewer keywords.

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4342437, C9303-7410D-077; 930203.

**Title**
Overview of unified simulation activity at **Mentor Graphics Corporation.**

**Author(s)**
Leef-S-A; Ed. by Luker-P.

**Author affiliation**
**Mentor Graphics** Corp, Wilsonville, OR, USA.

**S urce**
Proceedings of the 1992 Summer Computer Simulation Conference. Twenty-Fourth Annual Computer Simulation Conference, Reno, NV, USA, 27-30 July 1992, p.997-1001.
Sponsors: SCS.
Published: SCS, San Diego, CA, USA, 1992, xxii+1273 pp.

**Publication year**
1992.

**Language**
EN.

**Publication type**
CPP Conference Paper.

**Treatment codes**
G General or Review; P Practical.

**Abstract**
Simulation is an integral part of today's electronic design cycle. Multiple and heterogeneous design types and styles impose different sets of requirements onto individual simulators. The complex electronic systems frequently contain components that require concurrent analysis by several different simulators. This paper is an overview of the activity at **Mentor Graphics Corporation** aimed at addressing this problem by providing an environment where multiple, heterogeneous simulators can collaborate on a single design. (1 refs).

**Descriptors**
circuit-CAD; specification-languages.

**Keyw rds**
overview; hardware description language; unified simulation activity; **Mentor Graphics Corporation;** electronic design cycle; styles; simulators; complex electronic systems; concurrent analysis.

**Classification codes**
C7410D (Electronic engineering).
C6140D (High level languages).

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**Title**
A tool for developing functional models.

**Author(s)**
Arel-N; Savaria-Y; Ed. by Barnett-C-C; Holmes-W-M.

**Author affiliation**
Dept of Electr & Comput Eng, Ecole Polytech de Montreal, Que, Canada.

**Source**
Proceedings of the 1988 Summer Computer **Simulation** Conference, Seattle, WA, USA, 25-28 July 1988, p.626-31.
Sponsors: SCS.
Published: SCS, San Diego, CA, USA, 1988, xxxiv+960 pp.

**ISSN**
ISBN: 0-911801-38-3.

**Publication year**
1988.

**Language**
EN.

**Publication type**
CPP Conference Paper.

**Treatment codes**
P Practical.

**Abstract**
A tool for developing functional models of complex VLSI circuits has been developed and is described in this paper. This tool was developed to take advantage of the availability of good commercial logic simulators such as QUICKSIM from **Mentor Graphics.** The tool is a precompiler to BLM (Behavioral Language Model) offered as a means to develop functional models by **Mentor Graphics Corporation.** A simple HDL (hardware description language) was developed to simplify the task of rapidly producing functional descriptions. This HDL supports widely different levels of abstraction from very detailed switch descriptions to high level constructs such as multidimensional arrays. An important feature of the precompiler is its ability to do extensive consistency and error checking which are essential in a fast-turnaround model development process. (4 refs).

**Descriptors**

circuit-analysis-computing; logic-CAD; program-processors; specification-languages; VLSI.

**Keywords**

functional model development tool; abstraction levels; consistency checking; VLSI circuits; logic simulators; QUICKSIM; Behavioral Language Model; **Mentor Graphics Corporation;** hardware description language; functional descriptions; switch descriptions; multidimensional arrays; precompiler; error checking.

**Classification codes**

```
B1130B    (Computer-aided circuit analysis and design).
B2570     (Semiconductor integrated circuits).
C7410D    (Electronic engineering).
C5210B    (Computer-aided logic design).
C6150C    (Compilers, interpreters and other processors).
C6140D    (High level languages).
```